Lab Field-Programmable Gate Arrays

Initial Meeting

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July 26th, 2019

Design hardware implementation for Lucas-Kanade Optical Flow.

Implement design in VHDL.

Test implementation on FPGAs.

9 CP in track 'Intelligent Systems'

Prerequisites

Successful completion of DRS lecture

Programming skills in VHDL

Knowledge about FPGA hardware

Programming skills in Python are useful
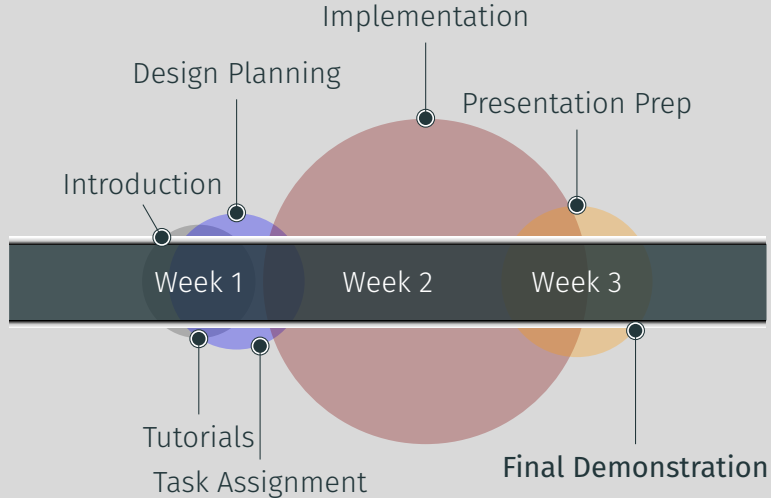
Organization

2-20 September, Mon-Fri, 9am - 5 pm

20 September – Final demonstration and presentation

8 seats – mail to `schueller@ti.uni-bonn.de`

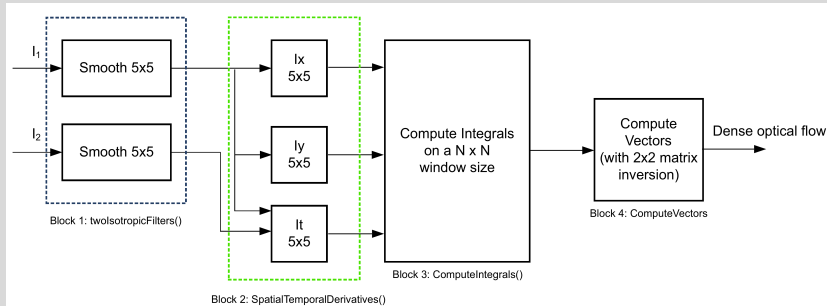Registration in BASIS – *2.9. - 4.9.*

Timeline

Implementation

Design Planning

Presentation Prep

Introduction

Week 1   Week 2   Week 3

Tutorials

Task Assignment

Final Demonstration

An Iterative Image Registration Technique with an Application to Stereo Vision
by Bruce D. Lucal and Takeo Kanade (1981)

Based on
Demystifying the Lucas-Kanade Optical Flow Algorithm with Vivado HLS
by Xilinx (2017)

Questions?